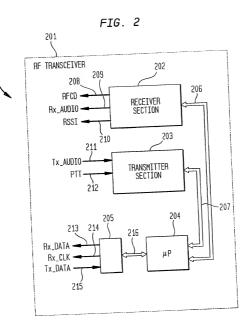
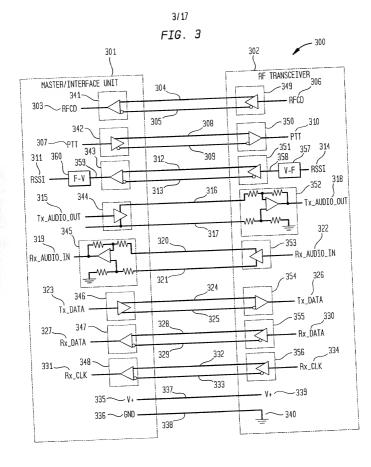


FIG. 1

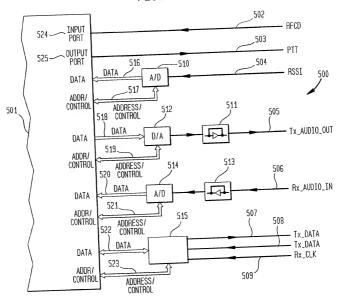
200



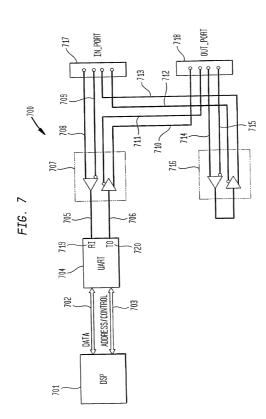


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FIG. 5



OUT_PORT IN_PORT -619 919/ -615 -614 612 611 622 FIG. 6 609 610 89 -604 624 2 623 H UART1 625 UART1 ADDRESS/CONTROL ADDRESS/CONTROL 909 602 - 109 DATA PATA 605 DSP 601





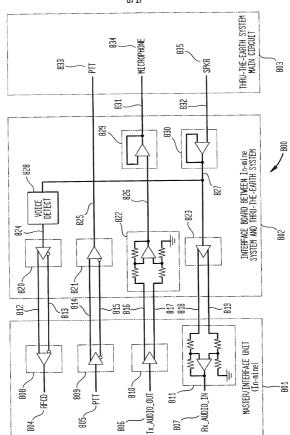
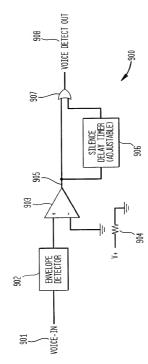


FIG. 9



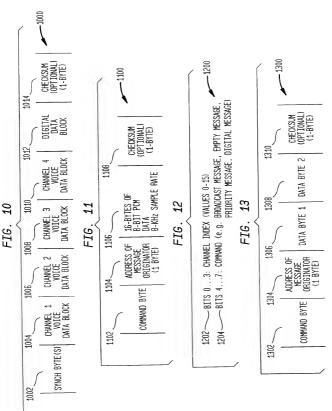


FIG. 14

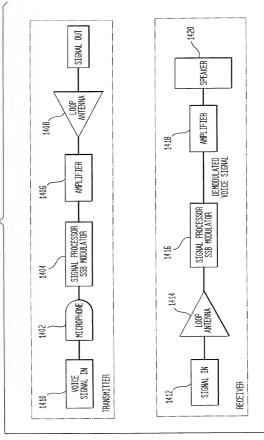
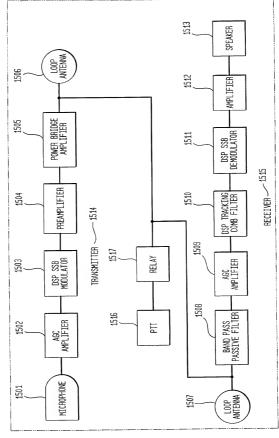


FIG. 15



BURNET HER TEST TEST TEST TO THE TEST OF THE

FIG. 16

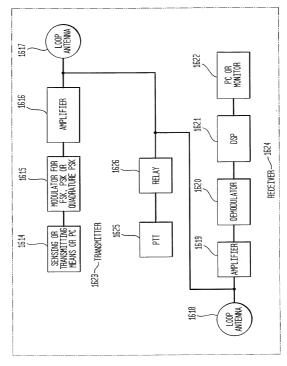


FIG. 17

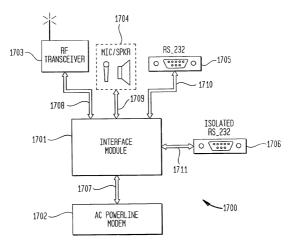
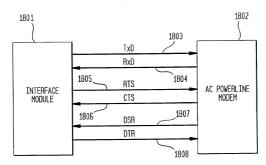
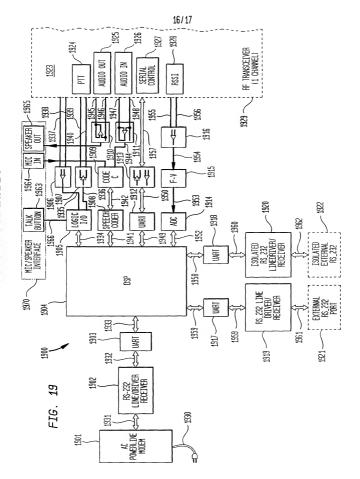
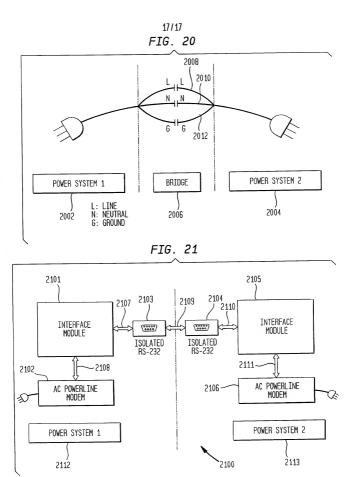


FIG. 18







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